

Program de masterat „Calculatoare”

Sisteme de calcul dedicate

Lucrarea de laborator Nr. 1. Proiectarea, programarea și simularea circuitelor combi-naționale temporizate în bază de dispozitive Microcontroler

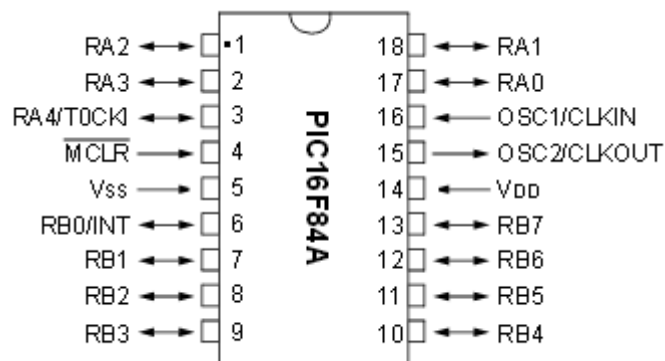
Scopul lucrării: Proiectarea, programarea și simularea circuitelor combi-naționale temporizate implementate în bază de dispozitive Microcontroler PIC16F84 destinate pentru gestiunea proceselor discret definite în timp real.

Surse și medii de proiectare:

- Mediul de proiectare a circuitelor electronice **ISIS Proteus**;
- Mediul de programare a dispozitivelor Microcontroler **IDE microC for PIC**;
- Mediul de simulare funcțională a produselor program **PIC Simulator IDE**.

Descrierea și argumentarea dispozitivului Microcontroler:

- Repartizarea și destinația pinilor:



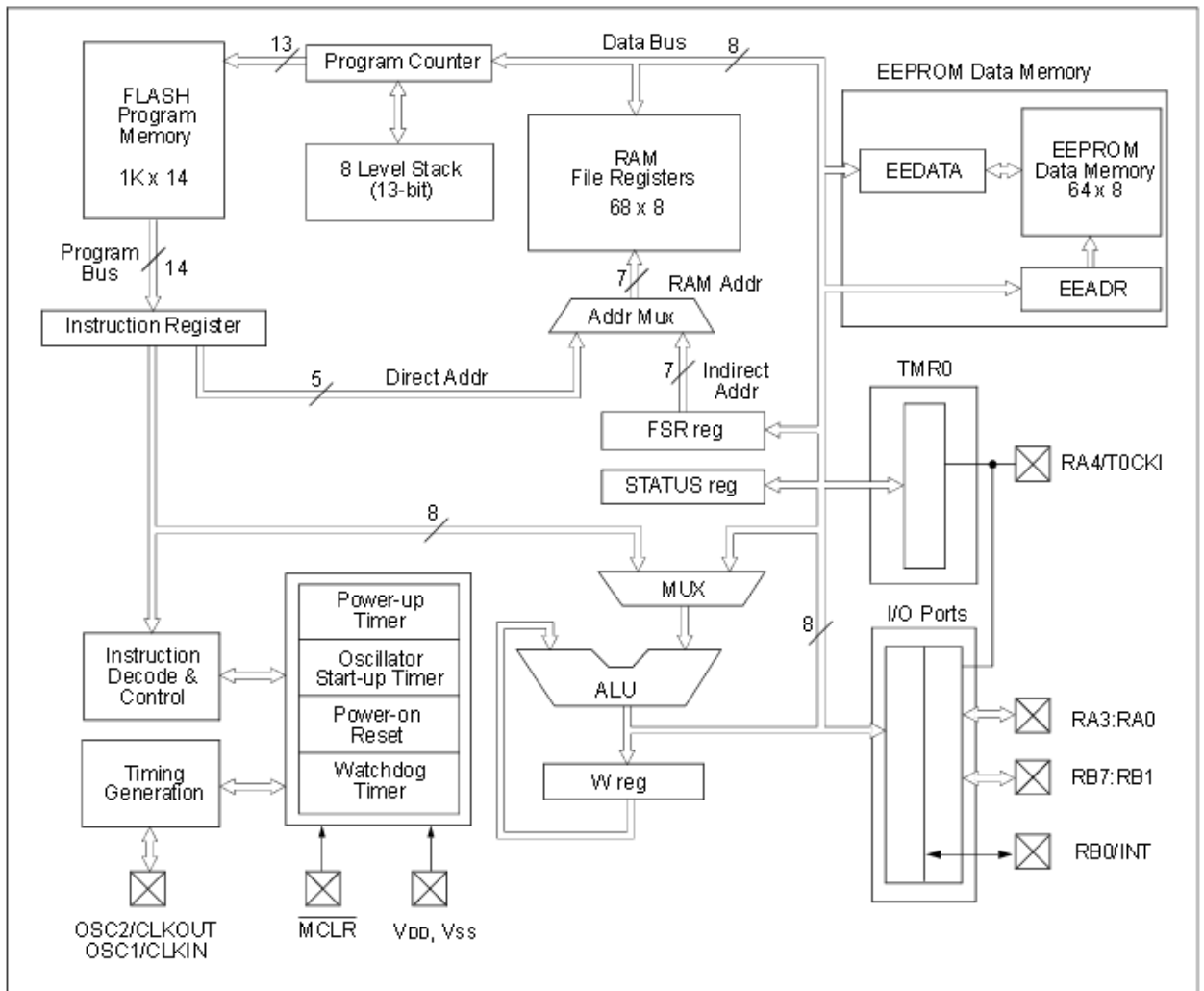
- Date caracteristice:

- Only 35 single word instructions to learn
- All instructions single-cycle except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input
DC - 200 ns instruction cycle
- 1024 words of program memory
- 68 bytes of Data RAM
- 64 bytes of Data EEPROM
- 14-bit wide instruction words
- 8-bit wide data bytes
- 15 Special Function Hardware registers
- Eight-level deep hardware stack
- Direct, indirect and relative addressing modes
- Four interrupt sources:
 - External RB0/INT pin
 - TMR0 timer overflow
 - PORTB<7:4> interrupt-on-change
 - Data EEPROM write complete

c) Echipamente periferice:

- 13 I/O pins with individual direction control
- High current sink/source for direct LED drive
 - 25 mA sink max. per pin
 - 25 mA source max. per pin
- TMR0: 8-bit timer/counter with 8-bit programmable prescaler

d) Structura interna a dispozitivului:



e) Descrierea funcțională a pinilor:

OSC1/CLKIN	16	16	18	I	ST/CMOS ⁽³⁾	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	15	19	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKOUT, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
MCLR	4	4	4	I/P	ST	Master Clear (Reset) input/programming voltage input. This pin is an active low RESET to the device.
RA0 RA1 RA2 RA3 RA4/T0CKI	17 18 1 2 3	17 18 1 2 3	19 20 1 2 3	I/O I/O I/O I/O I/O	TTL TTL TTL TTL ST	PORTA is a bi-directional I/O port. Can also be selected to be the clock input to the TMR0 timer/counter. Output is open drain type.
RB0/INT RB1 RB2 RB3 RB4 RB5 RB6 RB7	6 7 8 9 10 11 12 13	6 7 8 9 10 11 12 13	7 8 9 10 11 12 13 14	I/O I/O I/O I/O I/O I/O I/O I/O	TTL/ST ⁽¹⁾ TTL TTL TTL TTL TTL TTL/ST ⁽²⁾ TTL/ST ⁽²⁾	PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs. RB0/INT can also be selected as an external interrupt pin. Interrupt-on-change pin. Interrupt-on-change pin. Interrupt-on-change pin. Serial programming clock. Interrupt-on-change pin. Serial programming data.
Vss	5	5	5,6	P	—	Ground reference for logic and I/O pins.
Vdd	14	14	15,16	P	—	Positive supply for logic and I/O pins.

f) Descrierea funcțională a pinilor Portul RB:

Name	Bit	Buffer Type	I/O Consistency Function
RB0/INT	bit0	TTL/ST ⁽¹⁾	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3	bit3	TTL	Input/output pin. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB6	bit6	TTL/ST ⁽²⁾	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up. Serial programming clock.
RB7	bit7	TTL/ST ⁽²⁾	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger.

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

g) Descrierea setului de instrucțiuni:

Mnemonic, Operands	Description	Cycles	14Bit Opcode				Status Affected	Notes	
			MSb		LSb				
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	1fff	ffff	Z	2
CLRWF	-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1 (2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1 (2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	1fff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3
LITERAL AND CONTROL OPERATIONS									
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	$\overline{TO}, \overline{PD}$	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into standby mode	1	00	0000	0110	0011	$\overline{TO}, \overline{PD}$	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

Descrierea funcțională a circuitului logic combinațional temporizat:

Este definit sistemul de control implementat în baza MCU PIC16F84 (Figura 1). Sistemul include semnalele discrete de intrare RB[...] și semnalele discrete de ieșire RB[...].

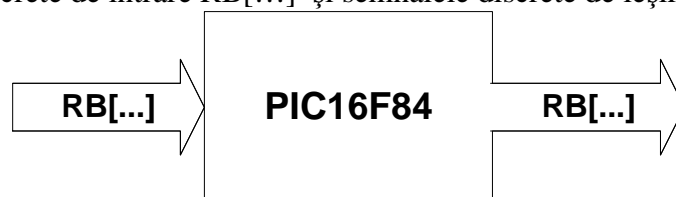


Figura 1.

- Să se elaboreze schema bloc a algoritmului de realizare a funcției logice **F**.
- Să se elaboreze programul în mediul **IDE microC for PIC** care realizează funcția logică **F**:

$$F = \begin{cases} RA.0 = 1, (\Delta t = 10ms) \left[(RB.0 \vee RB.2) \wedge RB.5 \right], \\ RA.1 = \overline{RA.1}, (\Delta t = 30ms) \left[(RB.0 \vee RB.3) \wedge (RB.2 \vee RB.7) \wedge (RB.1 \vee RB.4 \vee RB.5 \vee RB.6) \right], \\ RA.2 = 1, (\Delta t = 60ms) \left[(RB.2 \vee RB.3) \wedge \overline{(RB.3 \vee RB.6)} \wedge (RB.0 \vee RB.6 \vee RB.5 \vee RB.2) \right], \\ RA.4 = \overline{RA.2}, (\Delta t = 40ms) \left[(RB.1 \vee RB.2) \wedge (RB.2 \vee \overline{RB.4}) \wedge (RB.1 \vee RB.7 \vee RB.5) \right], \\ RA.1 = 1, (\Delta t = 120ms) \left[(RB.0 \vee \overline{RB.3}) \wedge \overline{(RB.0 \vee RB.7)} \wedge (RB.1 \vee \overline{RB.4} \vee \overline{RB.5 \vee RB.6}) \right]. \end{cases}$$

unde: Δt este timpul de întârziere a semnalului de control după îndeplinirea condiției menționate în [...].

Simularea funcțională a programului:

Rezultatul compilării programului ce realizează funcția logică F se verifică în mediul de simulare **PIC Simulator IDE**.